WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate;

an element isolation film formed such as to have a predetermined depth from a main surface of said semiconductor substrate, said element isolation film dividing the area from said main surface to said depth into a plurality of first regions;

first wells formed in said first regions, respectively; and

a second well formed in a second region deeper than said first wells in said semiconductor substrate, said second well being in contact with some of said first wells.

2. A semiconductor device according to claim 1 wherein said first and second wells of said first and second regions on one side with reference to a predetermined boundary are of a first conductivity type, and said first and [second wells] on the other side are of a second conductivity type.

3. A semiconductor device according to claim 2 wherein said second well of said first conductivity type and said second well of said second conductivity type are not in contact with each other.

4. A semiconductor device according to claim 1 wherein said second well is formed on only one side of said second region with reference to [a] said predetermined boundary.

5. A semiconductor device according to claim 4 wherein said second well is formed in a memory cell part in said second region.

6. A semiconductor device according to claim 1 wherein said second well is formed only in the vicinity of the bottom of said element isolation film in said second region.

fig. 15

7. A semiconductor device according to claim 1 wherein each impurity concentration of said first and second wells is higher as being closer to a boundary part between said first and second regions.

8. A semiconductor device according to claim 1 further comprising a third well formed in a third region deeper than said second region in said semiconductor substrate.

fig. 28

9. A method of manufacturing a semiconductor device comprising the steps of:

(a) forming an element isolation film such as to have a predetermined depth from a main surface of a semiconductor substrate, to divide the area from said main surface to said depth into a plurality of first regions; and

(b) forming first wells in said first regions, respectively, and forming a second well making contact with some of said first wells, in a second region deeper than said first wells in said semiconductor substrate.

10. A method according to claim 9 wherein said step (b) comprising the steps of:

(b-1) covering, with a first resist, one side region of said main surface with

reference to a predetermined boundary in said semiconductor substrate;

(b-2) implanting impurity of a first conductivity type into said first region by using said first resist as a mask;

(b-3) implanting impurity of the first conductivity type into said second region by using said first resist as a mask;

(b-4) removing said first resist;

(b-5) covering, with a second resist, the other side region of said main surface with reference to said boundary in said semiconductor substrate;

(b-6) implanting impurity of a second conductivity type into said first region by using said second resist as a mask;

(b-7) implanting impurity of the second conductivity type into said second region by using said second resist as a mask; and

(b-8) removing said second resist.

11. A method according to claim 9 wherein said step (b) comprising the steps of:

(b-1) covering, with a first resist, one side region of said main surface with reference to a predetermined boundary in said semiconductor substrate;

(b-2) implanting impurity of a first conductivity type into said first region by using said first resist as a mask;

(b-3) reforming said first resist such as to be thicker, as a second resist;

(b-4) implanting impurity of the first conductivity type into said second region by using said second resist as a mask;

(b-5) removing said second resist;

(b-6) covering, with a third resist, the other side region of said main surface

with reference to said boundary in said semiconductor substrate;

(b-7) implanting impurity of a second conductivity type into said first region by using said third resist as a mask;

(b-8) reforming said third resist such as to be thicker, as a fourth resist;

(b-9) implanting impurity of the second conductivity type into said second region by using said fourth resist as a mask; and

(b-10) removing said fourth resist.

12. A method of manufacturing a semiconductor device comprising the steps of:

(a) forming a trench such as to have a predetermined depth from a main surface of a semiconductor substrate, to divide the area from said main surface to said depth into a plurality of regions in said semiconductor substrate;

(b) implanting a first impurity from above said main surface into said trench; and

(c) implanting a second impurity from above said main surface into said regions.

add A2 add C5